IN THE DRAWINGS

Applicants enclose Annotated Sheets of Figs. 4 and 5 illustrating reference numeral corrections. Applicants also enclose corresponding Replacement Sheets for these figures reflecting the corrections.

REMARKS

Applicants cancel claims 7-8. Claims 1-6 remain pending in the application. Applicants amend Figs. 4-5 for minor corrections and claims 1-6 for clarification. Applicants refer to Figs. 4 and 10—and their corresponding description in the specification—for exemplary embodiments of and support for the claimed invention. No new matter has been added.

Applicants amend Figs. 4-5 to correct minor errors, and respectfully request that the Examiner accept the drawings.

The Examiner objected to claims 3-4 for unclear language. Applicants amend claims 3 and 4 to clearly recite the claimed feature of "an empty release," an exemplary embodiment of which is described in the specification with reference to Fig. 10 of the application. Applicants also amend claim 4 to clearly recite "said extracting part outputs said data signals in which an invalid data signal included in said input signal is deleted," as distinguished from the features of claim 3. Applicants also amend the claims to recite "storage state information" for clarity in accordance with the Examiner's suggestions. Accordingly, Applicants respectfully request that the Examiner withdraw the claim objections.

Claim 2 stands rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter of the invention.

In particular, the Examiner objected to claim 2 as being indefinite on "how the input signal is 'stored in an order of the first memory part, the second memory part, and the third memory part.'" Page 3, lines 4-6 of the Office Action. Applicants refer the Examiner to page 9, lines 1-24 of the specification for an exemplary embodiment of the claimed feature. Applicants respectfully request that the Examiner withdraw the § 112, ¶ 2 rejection.

Claim 1 stands rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,151,334 to Kim et al.; claims 3-5 and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim et al. in view of U.S. Patent No. 6,504,855 to Matsunaga; claim 6 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim et al. in view of U.S. Patent No. 6,874,048 to Knapp et al.; claim 2 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Kim et al. in view of U.S. Patent No. 6,721,295 to Brown; and claim 8 was rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,367,545 to Yamashita et al. Applicants cancel claims 7-8 and amend claims 1-6 in a good faith effort to clarify the invention as distinguished from the cited references. Applicants respectfully traverse the rejections.

Kim et al. describe a technique for sending multiple data signals over a serial link. And Matsunaga describes a multiplexer that is able to recognize valid and invalid data. Even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine Kim et al. and Matsunaga, the combination would, at most, have suggested the multiplexor 48 described in Kim et al. including a mechanism for recognizing valid and invalid data. Accordingly, a corresponding number of multiplexors 48 would be provided for as many input data signals for recognizing valid and invalid data. The combination would, therefore, have failed to disclose or suggest the single multiplexing circuit of the claimed invention.

In other words, Kim et al., as cited and relied upon by the Examiner do not disclose,

> "[a] device for processing data signals, comprising:
> a plurality of input interfaces each for inputting an input signal; and
> a multiplexing circuit for multiplexing a plurality of input signals from the plurality of input interfaces,

wherein said each of the plurality of input interfaces comprises:

a storing part storing the input signal; and

an extracting part extracting said data signals included in said input signal from said storing part and outputting said data signals at a desired output speed,

wherein said extracting part outputs said data signals based on storage state information of said input signal," as recited in claim 1. (Emphasis added)

Advantageously, the claimed invention provides for a technique where the state information of a middle storage unit may be used to adjust clock difference, and thus minimizing the loss of input data and/or output data even if a clock of a remote device is not synchronized.

Accordingly, Applicants respectfully submit that claim 1 is patentable over Kim et al. for at least the foregoing reasons. Applicants further submit that claims 3-5 and 7 dependent from claim 1 are patentable over Kim et al. and Matsunaga, separately and in combination, for at least the above-stated reasons. The Examiner cited Knapp et al., Brown, and Yamashita et al. to specifically address the additional features recited in dependent claims 6, 2, and 8, respectively. As such, the combinations with these references would still have failed to cure the above-described deficiencies of Kim et al., even assuming, arguendo, that such combinations would have been obvious to one skilled in the art at the time the claimed invention was made. Accordingly, Applicant respectfully submits that claims 2, 6, and 8 are patentable over the cited references for at least the above-stated reasons with respect to claim 1, from which they depend.

The above statements on the disclosure in the cited references represent the present opinions of the undersigned attorney. The Examiner is respectfully requested to specifically indicate those portions of the respective reference that provide the basis for a view contrary to any of the above-stated opinions.

Annotated Sheet

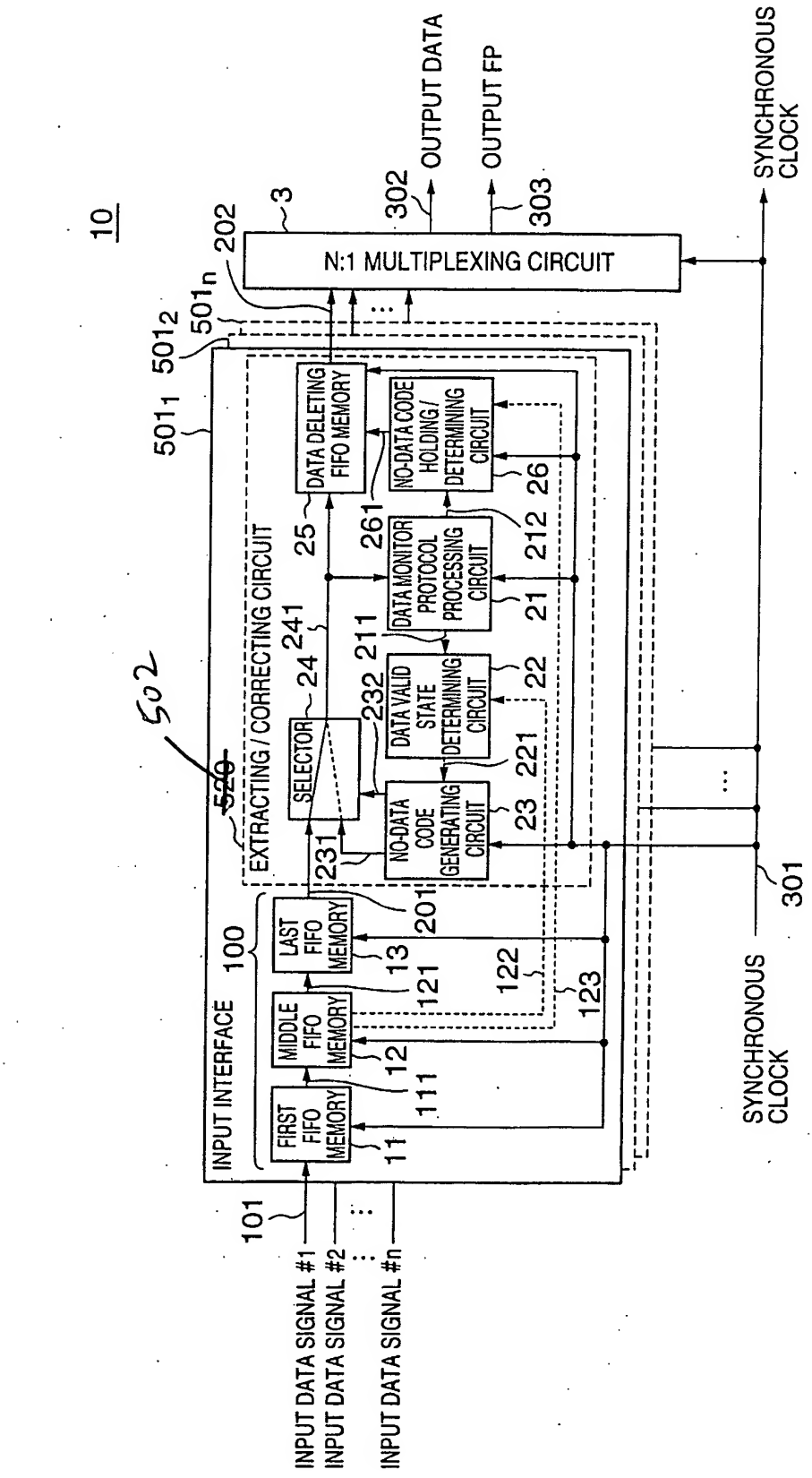

FIG.4

Annotated Sheet

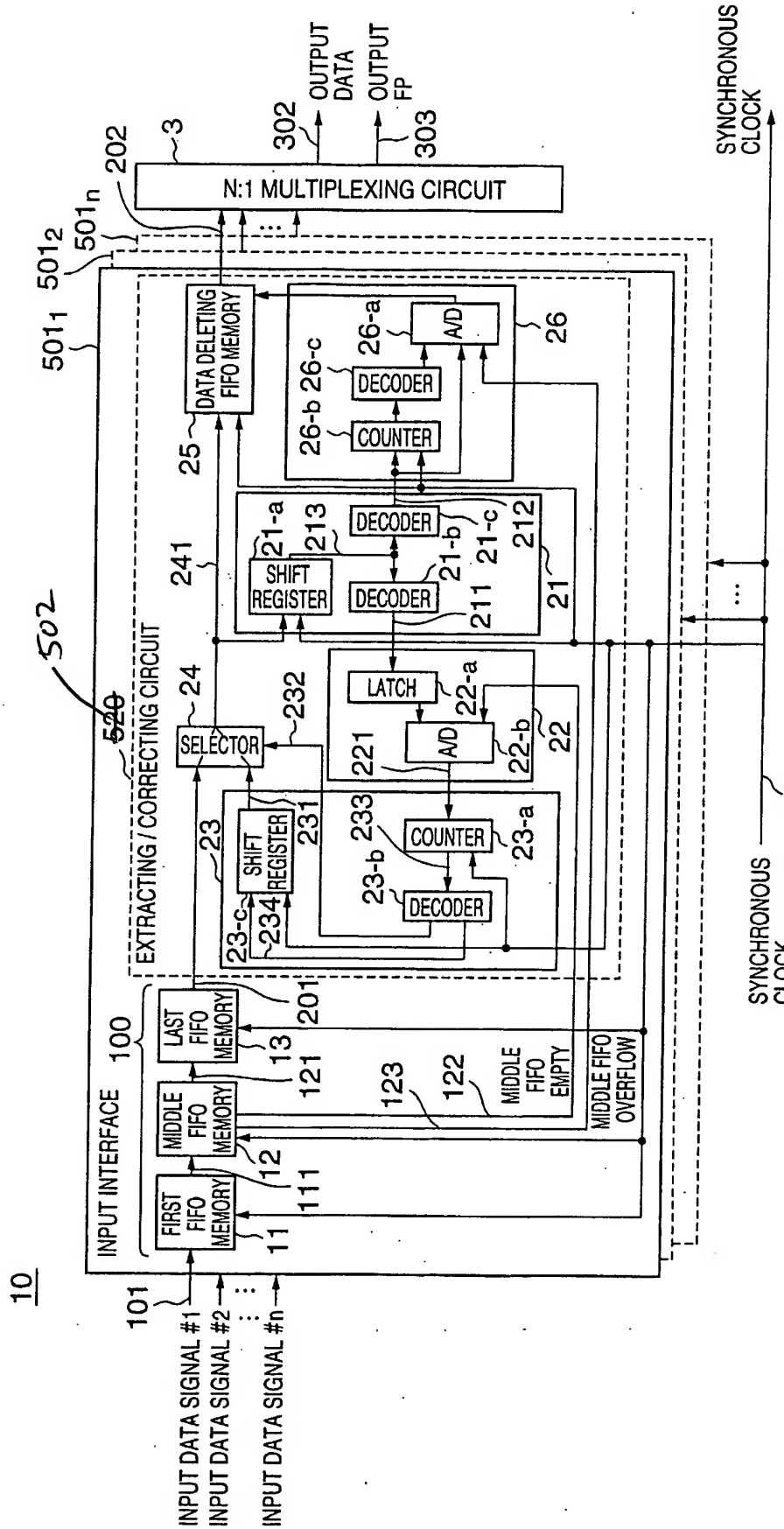

FIG.5